IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR:	Zhong-Ning (George) CAI
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TITLE:	METHOD AND APPARATUS FOR THERMAL SENSITIVITY BASED ON DYNAMIC POWER CONTROL
ART UNIT:	2116
EXAMINER:	Tse W. CHEN

Mail Stop Appeal Brief - Patents
Commissioner for Patents
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SUPPLEMENTAL REPLY BRIEF

SIR:

In response to the supplemental Examiner's Answer mailed June 9, 2006, this supplemental reply brief is respectfully submitted.

Remarks

Meaning of "performance demanding level input"

In paragraphs 2-5 on page 2 of the supplemental Examiner's Answer, the Examiner seeks to read out from the claims the meaning of "performance demanding level input" as "an input that relates to a level of performance of the processor in accordance with demand." In support of his position, the Examiner acknowledges that the disclosure describes a relation between the claimed

performance demanding level (PDL) input and a level of performance of the processor in accordance with demand, but argues that this meaning is only an "example" that cannot be read into the claims. Supplemental Examiner's Answer, page 2, 4th paragraph.

The Examiner errs. As stated in the MPEP, "[d]uring patent examination, the pending claims must be 'given their broadest reasonable interpretation *consistent with the specification*'" (emphasis added). MPEP 2111, citing *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). Here, the Examiner seeks to ignore those parts of the specification which do not support his position. The quoted authority does not grant the Examiner such leeway.

In any event, there need be no special resort to the specification to properly interpret the claims. The independent claims all recite a performance demanding level input to control a rate of frequency reduction of a processor or processor clock. The plain meaning of this language is not ambiguous: a performance demanding level of a processor is just that – it is a level at which a processor must perform in response to demand. The claimed performance demanding level input, therefore, controls a rate of processor clock frequency reduction in accordance with demand for performance. McDermott is simply silent as to any such control of processor frequency.

Even supposing the words "performance demanding level" were to be read out of the claims, the claims would still clearly distinguish over McDermott, since they would still recite an input that determines a rate of frequency reduction of a processor clock. The LVL1 and LVL2 signals of McDermott do not reduce a processor clock frequency; instead, they lock a PLL onto an input frequency so that the processor clock frequency does *not* change.

Nature of frequency changes in McDermott

The Examiner challenges the Appellant's assertion that the sole purpose of McDermott's invention is to ensure that the frequency of the system clock does not change. See supplemental Examiner's Answer, page 3, 2nd paragraph. In response, the Appellant reaffirms the Appellant's position that this is in fact the sole purpose of McDermott's invention.

As pointed out in McDermott, PLLs are conventionally implemented onto integrated circuits to overcome problems associated with high frequency clock signals, such as instabilities in the duty cycle, noise and ringing. See McDermott, col. 1, lines 37-45. To this end, the object of McDermott's invention is to "provide a fully-integrated charge pump PLL having a fast response time to input frequency changes as well as highly stable behavior in the phase-locked condition." McDermott, col. 2, lines 65-68.

Accordingly, the LVL1 and LVL2 inputs of McDermott are only to correct unavoidable frequency drift and lock onto the input frequency as quickly as possible, to *prevent* a clock frequency from changing. They are not designed to cause a clock's frequency to change, but to ensure that it does not. McDermott, therefore, offers no suggestion whatsoever with regard to reducing a processor frequency in accordance with demand for performance.

"Effective synchronization scheme"

The Examiner offers further comments on the "effective synchronization scheme" referred to in the previous Examiner's Answer. The comments actually bolster the Appellant's argument that McDermott in no way suggests frequency change in accordance with a performance demanding level input. Specifically, the Examiner further draws out the distinction between synchronization and frequency reduction in his comments: "An 'effective synchronization scheme' is important in a system of frequency reduction because any changes in frequency *ultimately requires synchronization* ..." Supplemental Examiner's Answer, page

3, 3rd paragraph. The Examiner therefore concedes that frequency reduction and synchronization are separate processes involving separate concerns. This serves to emphasize that the person skilled in the art, seeking to change frequency in accordance with demand for performance, would not look to techniques for synchronization of a PLL as are disclosed in McDermott. The Appellant reiterates that therefore the application of the McDermott reference is improper.

Conclusion

In view of the above, it is clear that the Examiner erred in finally rejecting claims 1-20. It is therefore respectfully requested that the Board reverse the Examiner and allow claims1-20.

The Examiner is invited to contact the undersigned at (202) 220-4323 to discuss any matter concerning this application. The Office is authorized to charge any fees related to this communication to Deposit Account No. 11-0600.

Respectfully submitted,

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